WHAT IS CLAIMED IS:

1. A formal equivalence verification method comprising:

characterizing an output of a circuit as a combinational function of a set of input values, wherein the values of the inputs that flow across signal paths are controlled by other signals.

2. The formal equivalence verification method of claim 1, wherein said circuit is a sequential circuit.

3. The formal equivalence verification method of claim 1, wherein each component of a circuit is provided with a corresponding mathematical representation.

4. The formal equivalence verification method of claim 1, wherein the mathematical expression is a Boolean representation.

5. The formal equivalence verification method of claim 4 wherein the Boolean expression is a Binary Expression Diagram (BED).

6. A formal equivalence verification method comprising:

computing a Timed Binary Expression Diagram (TBED) for each circuit node as a Binary Expression Diagram (BED); and

applying a satisfiability (SAT) solver or a binary decision diagram (BDD) tool to establish equivalence for each TBED corresponding to each circuit ouput node.

7. The formal equivalence verification method of claim 6, wherein the TBEDs of outputs of a specification circuit and an implementation circuit are compared.

8. The formal equivalence verification method of claim 7, wherein the circuit is a pipelined loop-free circuit.

9. A formal equivalence verification method comprising:

listing the latches in a predetermined order;

representing the latch functions in a binary format; and

computing a Timed Binary Expression Diagram (TBED) using a binary format.

10. The method of claim 9, wherein the binary format is a Binary Expression Diagram (BED) format.

11. The method of claim 9, wherein the TBED is converted into a format accepted by a Satisfiability (SAT) solver.

12. The method of claim 11, wherein if the SAT solver shows that the TBEDs of a plurality of circuits are equivalent then the circuits are equivalent as well.

13. The method of claim 12, wherein the equivalence determined by the SAT solver is a steady-state equivalence.

14. The method of claim 13, wherein the SAT solver determines combinational equivalence of Boolean formulas.

15. The method of claim 14, wherein the Boolean formulas comprise the TBEDs corresponding to specification and implementation outputs.

16. The method of claim 9, wherein the circuit latches are traversed in a predetermined order and the latches are traversed to build TBEDs.

17. The method of claim 16, wherein the predetermined order selected and traversed is a bottom-up order that moves from inputs towards outputs.

18. The method of claim 17, wherein a relevant latch list is traversed once, according to the predetermined order.

19. The method of claim 16, wherein the TBED accounts for combinational properties on circuit inputs as well as any internal circuit nodes imposed by the user.

20. A system for performing formal equivalence verification comprising a processor that defines a state transition for one or more latches in a circuit, places the latches in a predetermined order, represents the latches in a binary format, and computes a Timed Binary Expression Diagram (TBED) using a binary format.

21. The system of claim 20 wherein the TBED is converted into a format accepted by a Satisfiability (SAT) solver.

22. A computer readable media comprising:

code that lists the latches in a predetermined order;

code that represents the latch functions in a binary format; and

code that computes a Timed Binary Expression Diagram (TBED) using a binary format.

23. The computer readable media of claim 22, wherein the binary format is a Binary Expression Diagram (BED) format.

24. The computer readable media of claim 22, wherein the TBED is converted into a format accepted by a Satisfiability (SAT) solver.